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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Date: December 19, 2002

Misbahul Azam et al.

Serial No.: 09/705,274 Group Art Unit (2823)

Filed: November 3, 2000 Examiner: Khiem D. Nguyen

For: **TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY**

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APPEAL BRIEF

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Washington D.C. 20231

SIR:

Please consider the following Brief on Appeal for the above identified patent application assigned to Semiconductor Components Industries, L.L.C.

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I. REAL PARTY OF INTEREST

The subject application is assigned to SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C., the real party of interest.

II. RELATED APPEALS AND INTERFERENCES

To appellants' knowledge, there are no related appeals or interferences.

III. STATUS OF THE CLAIMS

1. Claims 1-25 remain in the application and are the claims on appeal. A copy of these claims is provided in Appendix A.

2. Claims 1-27 were filed with the original application.

3. In an office action mailed on February 14, 2002, claims 1-26 were rejected under 35 U.S.C. § 102(a) as being anticipated by Madson (U.S. Publication No. US2001/0049167 A1). Claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Madson in combination with Williams et al. (U.S. Patent No. 6,239,463). In an amendment dated May 14, 2002, claims 1, 2, 9, 17 and 25 were amended, and claims 26-27 were cancelled. A final rejection mailed on October 15, 2002, rejected claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over Madson in view of Williams et al.

IV. STATUS OF AMENDMENTS FILED SUBSEQUENT TO FINAL REJECTION

A response to the final rejection was submitted on September 17, 2002, but no claims were amended. An advisory action confirming the rejection of claims 1-25 was mailed on October 15, 2002, indicating that the application was not in condition for allowance. Subsequent to the advisory action, a Notice of Appeal was faxed October 25, 2002, concurrently with a Petition for Extension of Time under 37 C.F.R. §1.136(a) to extend the period for response to November 17, 2002.

IV. SUMMARY OF THE INVENTION

The present invention relates to a method of forming trenches in semiconductor devices. In one embodiment, a masking material (14) is disposed on the semiconductor device, and a protruding portion (18) is formed at a trench location by forming an opening (20) in the masking material adjacent to the trench location. A semiconductor material (24) is deposited to fill in the opening and the protruding portion is removed to form the trench (26). The semiconductor material is etched to round off corners (28) of the trench.

As described in the Background of the Invention, page 1, line 7, through page 2, line 15, during the process used to manufacture trench semiconductor devices, a dry plasma silicon etch step typically is used to form the trenches in a silicon material. These processes must precisely control depth and not damage the channel region which is formed

along the trench wall. Such damage can cause leakage and reduced carrier lifetime in the channel area, thereby increasing the voltage threshold and on-state resistance of the semiconductor device. The trench depth typically is a critical dimension which is difficult to control using dry silicon etch processes. For example, a trench power MOSPET device should have the trench depth just below the diffused body region to minimize the gate to drain capacitance and minimize the gate oxide electric field strength.

Applicants found that by using a dielectric masking material (18) such as an oxide or nitride to define a trench (26), depositing semiconductor material (24) in openings in the masking material, removing the masking material to form the trench (using a simple non-damaging mask removal process) produces a trench having a precisely controlled depth free of wall damage, as well as not disturbing dopants (30) along the sidewall channel region. The controlled trench depth and substantially damage free channel region improve the electrical performance of the semiconductor device. Additionally, a simple wet etch trench rounding process is performed to round the corners of the trench above the foundation layer (12) to reduce field stress.

VI. ISSUE

Whether claims 1-25 are patentable under 35 U.S.C. § 103(a) over Madson (U.S. Publication No. U.S. 2001/0049167 A1) in view of Williams et al. (U.S. 6,291,298 B1).

VII. GROUPING OF THE CLAIMS

Appellants offer no other grouping of claims.

VIII. ARGUMENT

The Examiner rejected Claims 1-25 under 35 U.S.C. §103(a) over Madson in view of Williams et al. (Williams).

Claim 1 recites a method of forming a trench in a semiconductor device, comprising, among other things, forming a protruding portion (18) in a masking material (14), depositing a semiconductor material (24), removing the protruding portion to form the trench, and etching the semiconductor material to round off corners of the trench.

The Madson reference discloses several methods of manufacturing a trench transistor in which a semiconductor material (figure 8A, 802) is deposited in a region defined by a dielectric pillar (figure 8B, 806). The height of the dielectric pillar is reduced by plasma etching to leave a shorter dielectric pillar, i.e., a dielectric plug ("OX" of Fig. 8D) of a predetermined thickness (reference paragraphs 0007, 0010, 0011, 0013, 0014, 0028, 0035, 0039, 0041, 0044, 0056, 0058, 0060, 0062 and 0070). The Madson trench (i.e., figure 8D, 810) is formed over the shortened dielectric pillar (figure 8D, "OX").

The Williams reference discloses a method of forming a trench device wherein the trench is formed with rounded corners in an epi layer by isotropic and anisotropic plasma etching. That is, the Williams trench is formed in the foundation layer (N-epi layer) to limit damage to a subsequently formed gate oxide layer (c5, lines 13-35).

The references, either alone or when combined, do not disclose the invention as claimed. In particular, neither reference discloses, teaches or suggests a step of removing a protruding portion of a masking material to form a trench. The Madson reference reduces the height of, but does not

remove, protruding dielectric pillar 806 to form a reduced height dielectric pillar or dielectric plug OX (FIG. 8D). All of the Madson devices are shown having the trench terminating on the top of dielectric plug OX. Nowhere in the Madson specification is any teaching provided or suggestion made to remove the dielectric pillar rather than reduce its height. Reducing the height of a dielectric pillar is not the same as removing a protruding portion of a masking material.

The Williams reference forms a trench by removing a portion (212) of epitaxial semiconductor material (epi), not masking material. Moreover, because all of the Williams devices are formed by etching semiconductor material (n epi, n epi layer 108) to form the trench, there is no etch stop that allows precise control of the trench depth. In contrast, the claimed device removes a protruding portion of masking material so that the underlying material provides an etch stop that results in a trench with a precisely controlled depth, as described on page 5, lines 23-34 of the specification.

Therefore, the references, either alone or in combination, do not disclose the claimed invention.

Furthermore, Madson in view of Williams fails to make claim 1 obvious because one skilled in the art would not be motivated to combine them. Obviousness cannot be established by combining the teaching of the prior art to produce the claimed invention absent, among other things, incentive supporting the combination. ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1576, 221 USPQ 929, 933 (Fed. Cir. 1984). When a 35 U.S.C. § 103 rejection is based upon a modification of a reference that destroys the intent or purpose of the invention disclosed in the

reference, such a proposed modification is not proper and a prima facie case of obviousness cannot be properly made.

There is no motivation in the Madson reference to perform a step of etching the trench to round off corners of the trench, and in fact the reference is silent with respect to rounding of trench corners. It is well accepted that silence in a reference is not a proper substitute for an adequate disclosure of facts from which a conclusion of obviousness may justifiably follow.

In order to round the corners of the Madson trench, the shortened dielectric pillar would have to be removed to prevent any rounding process from forming voids detrimental to device operation along the sides of the shortened dielectric pillar. If anything, Madson teaches away from removing a protruding portion of masking material. Thus, applicants respectfully submit that Madson fails to make claim 1 obvious.

The shortened dielectric pillar allows the Madson device to achieve a high breakdown voltage and low or predetermined drain to gate capacitance without removing the shortened dielectric pillar. Since the objectives of the Madson device are achieved by leaving the shortened dielectric pillar in the trench, there would be no motivation to add processing steps to remove the shortened dielectric pillar to round off corners of the trench because such steps would add cost and would increase the drain to gate capacitance and reduce control over its value, effectively defeating one purpose of the Madson device.

Hence, there is no incentive to combine the Madson and Williams references. Such combining would destroy the purpose of the Madson invention to form a trench terminating on top of a shortened dielectric pillar to increase

breakdown voltage and decrease or better control drain to gate capacitance. In order to round the corners of the Madson trench, the shortened dielectric pillar would have to be removed or else voids would form along the sides of the shortened dielectric pillar. In effect, the Madson reference teaches away from a rounding etch by disclosing the trench etch terminating on the top of a shortened dielectric pillar (¶¶ [0007], [0028], [0044]).

Since the objectives of the Madson device are achieved by leaving the shortened dielectric pillar in the trench, there would be no motivation to add processing steps to remove the shortened dielectric pillar from the trench because such a step would effectively defeat one purpose of the Madson device. More processing steps would then be needed to incorporate the Williams et al. etch step to round off corners of the trench to provide the high breakdown voltage that was already present with the oxide pillar.

Finally, even if the Madson device were combined with the Williams et al. device and voids were not produced along the sides of the dielectric plug, the result would be a device having a protruding plug of oxide left from the pillar in the bottom of the trench, and would not have the advantage taught by the applicant of improved depth control, breakdown improvements and accurate alignment of the trench bottom to the foundation layer (12) as described in the specification on page 7, line 15 through page 9, line 24. Furthermore, such a device would not have the rounded off semiconductor material on top of a foundation layer 12 as does the applicant. Instead, the rounding would occur on top of the Madson plug resulting in poor channel resistance.

Therefore, Applicants respectfully submit that combining Madson with Williams would destroy the intent of the Madson invention.

The Examiner further states it would have been obvious to "combine the teachings of Williams with the method of Madson to help reduce the strength of the electrical field near the bottom of the trench". However, the Examiner has not shown any basis in either Madson or Williams for combining or modifying either references support such a statement. Since the intended function of the Madson device would be destroyed if the shortened dielectric pillar were removed, Applicants submit that there is no such motivation.

Thus, the combination of the Madson and Williams references do not show or teach a method of forming a trench in a semiconductor device, comprising, among other things, forming a protruding portion in a masking material, depositing a semiconductor material, removing the protruding portion to form the trench, and etching the semiconductor material to round off corners of the trench as does the applicant.

For at least the above reasons, applicants respectfully submit that Madson in view of Williams does not make claim 1 obvious.

Claims 2-8 depend from claim 1 and is believed allowable for at least the same reasons as claim 1.

Claim 9 calls for, among other things, a method of forming a trench in a semiconductor device comprising removing a protruding region to form a trench within a second epi layer and etching the second epi layer to round off corners of the trench.

Claim 9 is believed allowable for reasons similar to those set forth in claim 1 above. Claims 10-16 depend from claim 9 and are believed allowable for at least the same reasons as claim 9.

Claim 17 calls for, among other things, a method of forming a trench in a semiconductor device comprising removing a protruding region to form the trench and etching a second material to round off corners of the trench.

Claim 17 is believed allowable for similar reasons as those discussed in claim 1 as set forth above. Claims 18-25 depend from claim 17 and are believed allowable for at least the same reasons as claim 1.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,
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APPENDIX A

Claims

1. A method of forming a trench in a semiconductor device, comprising:

disposing a masking material on the semiconductor device;

forming a protruding portion at a location of the trench by forming an opening in the masking material adjacent to the location of the trench;

depositing a semiconductor material to fill in the opening;

removing the protruding portion to form the trench; and

etching the semiconductor material to round off corners of the trench.

2. The method of claim 1, further including:

providing a substrate supporting the masking material; and

forming a first epi layer between the substrate and the masking material.

3. The method of claim 1, wherein the semiconductor material is an epitaxial material.

4. The method of claim 1, further including the step of forming a mask at the location of the trench after disposing the masking material.

5. The method of claim 4, wherein forming the protruding portion further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

6. The method of claim 1, wherein depositing the semiconductor material includes using a selective epi growth process to fill in the opening.

7. The method of claim 1, wherein depositing the semiconductor material includes using a blanket epi growth process to deposit the semiconductor material over the protruding portion and in the opening.

8. The method of claim 1, wherein removing the protruding portion step is a non-damaging mask removal step.

9. A method of forming a trench in a semiconductor device, comprising:

providing a substrate for the semiconductor device;

forming a first epi layer above the substrate and having a major surface;

forming a protruding region on the first epi layer having an opening adjacent to the protruding region and exposing the major surface of the first epi layer;

forming a second epi layer within the opening adjacent to the protruding region;

removing the protruding region to form the trench within the second epi layer aligned with the major surface of the first epi layer of the semiconductor device; and

etching the second epi layer to round off corners of the trench.

10. The method of claim 9, further including before forming the protruding region, forming a masking material above the first epi layer.

11. The method of claim 10, further including forming a mask on the masking material at a location for the trench;

12. The method of claim 11, wherein the mask is a photoresist material.

13. The method of claim 11, wherein forming the protruding region further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

14. The method of claim 9, wherein forming the second epi layer includes using a selective epi growth process.

15. The method of claim 9, wherein forming the second epi layer further includes forming the second epi layer over the protruding region.

16. The method of claim 15, wherein forming the second epi layer over the protruding region includes using a blanket epi growth process.

17. A method of forming a trench in a semiconductor device, comprising;

disposing a first material on the semiconductor device;

forming first and second openings in the first material to form a protruding region;

disposing a second material in the first and second openings;

removing the protruding region to form the trench; and

etching the second material to round off corners of the trench.

18. The method of claim 17, further including:

forming a substrate below the first material; and

forming an epi layer between the substrate and the first material.

19. The method of claim 17, wherein the first material is a masking material from a group consisting of silicon dioxide and silicon nitride.

20. The method of claim 17, wherein the second material is an epitaxial material comprised of silicon.

21. The method of claim 17, further including forming a mask on the first material after disposing the first material.

22. The method of claim 21, wherein forming the first and second openings includes performing an etch step to remove the first material adjacent to the mask.

23. The method of claim 17, wherein disposing the second material includes using a selective epi growth process.

24. The method of claim 17, wherein disposing the second material further includes disposing the second material over the protruding region.

25. The method of claim 24, wherein disposing the second material over the protruding region includes using a blanket epi growth process.